What is claimed is:

1. A method of fabricating a metal oxide semiconductor field effect transistor (MOSFET), comprising:

providing a substrate comprising a layer of strained silicon grown on a layer of silicon germanium;

providing a mask on the strained silicon layer that defines exposed areas in which shallow trench isolations are formed;

performing ion implantation in the exposed areas to damage the strained silicon in the exposed areas;

etching the strained silicon and the silicon germanium in the exposed areas to form trenches;

forming shallow trench isolations in the trenches; and

forming a MOSFET comprising the strained silicon layer in an active area defined by the shallow trench isolations.

2. The method claimed in claim 1, wherein ion that is implanted to damage the strained silicon is one of silicon, germanium, argon, xenon and nitrogen.

3. The method claimed in claim 1, wherein the first silicon germanium layer has a composition $Si_{1-x}Ge_x$, where x is in the range of 0.1 to 0.3.

4. The method claimed in claim 1, wherein forming said MOSFET comprises:

forming a gate insulating layer on the strained silicon layer;

forming a gate conductive layer on the gate insulating layer;

patterning the gate conductive layer and the gate insulating layer to form a gate overlying a gate insulator.

5. The method claimed in claim 4, wherein forming said MOSFET further comprises:

forming a first spacer around the gate and gate insulator; and

implanting shallow source and drain extensions.

6. The method claimed in claim 5, wherein implanting shallow source and drain extensions is preceded by implanting halo regions, the halo regions extending toward a channel region beyond ends of the source and drain extensions to be formed, the halo regions comprising a dopant having a conductivity type opposite to the conductivity type of a dopant of the source and drain extensions.

7. The method claimed in claim 6, wherein forming the MOSFET further comprises:

forming a second spacer around the first spacer; and

implanting deep source and drain regions,

wherein the second spacer serves as an implantation mask during implanting of the deep source and drain regions.

8. The method claimed in claim 7, wherein forming the MOSFET further comprises:

forming silicide source and drain contacts and a silicide gate contact.

9. The method claimed in claim 8, wherein the silicide source and drain contacts and the silicide gate contact comprise nickel.

10. The method claimed in claim 8, wherein forming silicide source and drain contacts and a silicide gate contact is preceded by annealing to activate implanted dopants.

11. The method claimed in claim 1, wherein providing the substrate comprises growing layer of silicon germanium on a semiconductor substrate

12. The method claimed in claim 11, further comprises growing a layer of strained silicon on the layer of silicon germanium

13. The method claimed in claim 12, wherein the layer of silicon germanium and the layer of strained silicon are grown together in a single continuous in situ deposition process.

14. The method claimed in claim 1, wherein said mask comprises a bi-layer hardmask.

15. The method claimed in claim 14, wherein the mask comprises a photoresist mask that is left in place during said ion implantation

16. The method claimed in claim 1, wherein providing said mask comprises

forming a layer of silicon oxide on the layer of strained silicon; and

forming a layer of silicon nitride on the layer of silicon oxide.

17. The method claimed in claim 16, wherein providing the mask further comprises:

patterning the layer of silicon nitride and the layer of silicon oxide using a photoresist mask.

18. The method claimed in claim 17, wherein the photoresist mask is left on the layer of silicon nitride during said ion implantation

19. A MOSFET device formed in accordance with the method recited in claim 1.

20. A method of fabricating a metal oxide semiconductor field effect transistor (MOSFET), comprising:

providing a substrate comprising a layer of strained silicon grown on a layer of silicon germanium;

providing a mask on the strained silicon layer that defines exposed areas in which shallow trench isolations are formed, the mask comprising a bi-layer hardmask and a photoresist mask;

performing ion implantation in the exposed areas to damage the strained silicon in the exposed areas, wherein the photoresist mask is left in place during said ion implantation to protect said bi-layer hardmask;

etching the strained silicon in the exposed areas and the silicon germanium layer beneath the exposed areas to form trenches;

forming shallow trench isolations in the trenches; and

forming a MOSFET comprising the strained silicon layer in an active area defined by the shallow trench isolations.

21. A MOSFET device formed in accordance with the method recited in claim 20.

22. A method of fabricating a metal oxide semiconductor field effect transistor (MOSFET), comprising:

providing a substrate comprising a layer of strained silicon grown on a layer of silicon germanium;

etching the strained silicon layer and the silicon germanium layer to form trenches;

forming shallow trench isolations in the trenches;

forming a gate and gate insulator on the strained silicon layer;

implanting shallow source and drain extensions;

implanting deep source and drain regions; and

forming silicides on the gate and the source and drain regions,

wherein etching of the strained silicon layer and silicon germanium layer to form trenches is preceded by implanting ions in the strained silicon in the regions of said trenches to reduce undercutting of the silicon germanium layer during etching of said trenches.

23. A MOSFET device formed in accordance with the method recited in claim 22.